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C. Amendments to the Claims.

1. **(Currently Amended)** A semiconductor device including an insulated gate field effect transistor (IGFET), comprising:

a gate electrode of the IGFET having a lower layer electrode formed on a gate insulating film and an upper layer electrode formed on the lower layer electrode;

a cap film formed on the upper layer electrode;

a first nitride film on a side surface of the upper layer electrode;

an oxide film on a side surface of the lower layer electrode; and

an etching stopper film including a second nitride film formed on the outside of the first nitride film and an outside surface of the oxide film

wherein the first nitride film has a film thickness of approximately 2 to 5 nm **and the first nitride film does not cover the side surface of the cap film.**

2. (Original) The semiconductor device according to claim 1, wherein:

first nitride film is a thermal nitride film.

3. (Original) The semiconductor device of claim 2, wherein:

first nitride film is a rapidly heated thermal nitride film.

Claim 4. (Cancelled)

5. (Original) The semiconductor device of claim 2, further including:

an interlayer insulating film formed to cover the gate electrode of the IGFET;

a contact hole opened in the interlayer insulating film to expose a source/drain region of the IGFET; and

a conductor filling the contact hole and electrically connected with the source/drain region.

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6. (Original): The semiconductor device of claim 2, wherein:

the oxide film is a thermal oxide film.

7. (Original): The semiconductor device of claim 2, wherein:

the second nitride film is formed with chemical vapor deposition (CVD).

Claims 8-16. (Cancelled)

17. (Previously Presented) A semiconductor device including a first region and a second region, comprising:

a first gate electrode of a first IGFET in the first region having a first lower layer electrode formed on a first gate insulating film and a first upper layer electrode formed on the first lower layer electrode;

a first cap film formed on the first upper layer electrode;

a first nitride film on a side surface of the first upper layer electrode that does not cover the side surface of the first cap film;

a first oxide film on a side surface of the first lower layer electrode;

a first etching stopper film including a second nitride film formed on the outside of the first nitride film and first oxide film;

a second gate electrode of a second IGFET in the second region having a second lower layer electrode formed on a second gate insulating film and a second upper layer electrode formed on the second lower layer electrode;

a second cap film formed on the second upper layer electrode;

a third nitride film on a side surface of the second upper layer electrode that does not cover the side surface of the second cap film;

a second oxide film on a side surface of the second lower layer electrode;

a second etching stopper film including a fourth nitride film formed on the outside of the third nitride film and second oxide film; and

wherein the first IGFET includes a lightly doped drain and the second IGFET does not include a lightly doped drain.

18. (Previously Presented) The semiconductor device of claim 17, wherein:

the semiconductor device is a semiconductor memory device; and

the first and second nitride films have a thickness of less than 6 nm.

19. (Original) The semiconductor device of claim 18, wherein:

the first region is a memory cell region and the second region is a peripheral circuit region.

20. (Original) The semiconductor device of claim 19, further including:

a first contact providing an electrical connection to a first source/drain region of the first IGFET;

a second contact providing an electrical connection to a second source/drain region of the second IGFET; and

a first spacing from the first contact to the first gate electrode is greater than a second spacing from the second contact to the second gate electrode.

21. (**Currently Amended**) A semiconductor device, comprising:

a first transistor formed in a first region comprising

a first upper layer gate electrode formed on and in electrical connection with a corresponding first lower layer gate electrode,

a first insulating film formed on a **majority of a** side surface of the first lower layer gate electrode ~~**and not on the side surface of the first upper layer gate electrode**~~,

a second insulating film formed on a side surface of the first upper layer gate electrode, the second insulating film having a lower thermal growth rate with respect to the first upper layer gate electrode material than the thermal growth rate

of the first insulating film with respect to the first lower layer gate electrode material, and

a first etching stopper film formed on the outside of the first and second insulating films **and in contact with a majority of an outside surface of the first insulating film formed on the majority of the side surface of the first lower layer gate electrode**

wherein the second insulating film has a thickness of less than 6 nm.

22. (Previously Presented) The semiconductor device of claim 21, wherein:

the second insulating film comprises a thermal nitride film.

23. (Previously Presented) The semiconductor device of claim 21, wherein:

the first insulating film comprises a thermal silicon dioxide film.

24. (Previously Presented) The semiconductor device of claim 21, wherein:

the etching stopper film comprises a chemical vapor deposition silicon nitride film.

25. (Previously Presented) The semiconductor device of claim 21, wherein:

the first lower layer gate electrode has a greater gate length than the first upper layer gate electrode.

26. (Previously Presented) The semiconductor device of claim 21, further including:

a second transistor formed in a second region comprising

a second upper layer gate electrode formed on and in electrical connection with a corresponding second lower layer gate electrode,

a third insulating film formed on a side surface of the second lower layer gate electrode and not on the side surface of the second upper layer gate electrode,

a fourth insulating film formed on a side surface of the second upper layer gate electrode, the fourth insulating film having a lower thermal growth rate with

respect to the second upper layer gate electrode material than the thermal growth rate of the third insulating film with respect to the second lower layer gate electrode material,

a second etching stopper film formed on the outside of the third and fourth insulating films,

a first transistor source/drain region extending laterally below the second etching stopper film, and

a second transistor source/drain region overlapping a portion of the first transistor source region that does not extend laterally below the second etching stopper film.

27. (Previously Presented) The semiconductor device of claim 26, further including:

a third transistor source/drain region having a different concentration than either the first or second transistor source/drain regions extending laterally below the first etching stopper film.

28. (Currently Amended) ~~The~~A semiconductor device ~~of claim 27, further including~~comprising:

a first transistor formed in a first region comprising

a first upper layer gate electrode formed on and in electrical connection with a corresponding first lower layer gate electrode,

a first insulating film formed on a side surface of the first lower layer gate electrode and not on the side surface of the first upper layer gate electrode,

a second insulating film formed on a side surface of the first upper layer gate electrode, the second insulating film having a lower thermal growth rate with respect to the first upper layer gate electrode material than the thermal growth rate of the first insulating film with respect to the first lower layer gate electrode material, and

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a first etching stopper film formed on the outside of the first and second insulating films wherein the second insulating film has a thickness of less than 6 nm;

a second transistor formed in a second region comprising

a second upper layer gate electrode formed on and in electrical connection with a corresponding second lower layer gate electrode,

a third insulating film formed on a side surface of the second lower layer gate electrode and not on the side surface of the second upper layer gate electrode,

a fourth insulating film formed on a side surface of the second upper layer gate electrode, the fourth insulating film having a lower thermal growth rate with respect to the second upper layer gate electrode material than the thermal growth rate of the third insulating film with respect to the second lower layer gate electrode material,

a second etching stopper film formed on the outside of the third and fourth insulating films,

a first transistor source/drain region extending laterally below the second etching stopper film, and

a second transistor source/drain region overlapping a portion of the first transistor source region that does not extend laterally below the second etching stopper film;

a third transistor source/drain region having a different concentration than either the first or second transistor source/drain regions extending laterally below the first etching stopper film;

the first transistor includes at least a third transistor source/drain region;

a first contact in electrical connection with the third source/drain region, and isolated from the first lower layer gate electrode by a first insulating thickness; and

a second contact in electrical connection with the first and second source/drain regions, and isolated from the second lower layer gate electrode by a second insulating thickness that is greater than the first insulating thickness.

29. **(Cancelled)** The semiconductor device of claim 1, wherein:

the first nitride film does not cover the side surface of the cap film.